Workshop "Accelerated Computing for Fusion" ***v4a***

November Tue 28 & Wed 29, 2017 - amphi 34, Maison de la Simulation, Saclay, France

Session	Start	Duration	End	Speaker	Org	Title
	08:45	00:05	08:50			Intro Tuesday morning
Hardware vendors & experts	08:50	00:25	09:15	G.ColinDeVerdière	CEA/DIF	Processors Roadmaps
Computing center experience	09:15	00:25	09:40	J.Noe	CEA/DRF	**helios** experience
Computing center experience	09:40	00:25	10:05	P.Lanucara	CINECA	CINECA **marconi** experience & perspectives
Computing center experience	10:05	00:20	10:25	Y.Ishii/N.Miyato	QST	Current Rokkasho HPC status
	10:25	00:20	10:45			*--Coffee break*
Hardware vendors & experts	10:45	00:25	11:10	G.Hautreux	GENCI	GENCI's Technology watch experience
Academics	11:10	00:25	11:35	M.Lobet	MdlS	Pic Codes on the road to Exascale : adaptation to MIC architectures
User's accelerator experience	11:35	00:25	12:00	N.Moschuering	IPP/HLST	HLST project CINCOMP3
User's accelerator experience	12:00	00:25	12:25	Y.Asahi	CEA/DRF&JAEA	Experience with GYSELA & accelerators
	12:25	00:00	12:25			*--End of day 1 / Adjourn to next day*
	08:40	00:05	08:45			Intro Wednesday morning
HPC prospective vision for fusion	08:45	00:30	09:15	M.Yagi	QST	Benchmark of Reduced MHD code using KNC and KNL
HPC prospective vision for fusion	09:15	00:30	09:45	S.Satake	Tokyo U of Science	Direct Numerical Simulation of Turbulent Shear Flow by MPI+OpenMP for Heterogeneous Computing Using Multi-CPU and Multi-MIC
HPC prospective vision for fusion	09:45	00:30	10:15	L.Villard	EPFL	European fusion HPC experience & perspective
	10:15	00:20	10:35			*--Coffee break*
Hardware vendors & experts	10:35	00:25	11:00	E.Petit	Intel	Intel HPC perspective
Hardware vendors & experts	11:00	00:25	11:25	F.Courteille	NVIDIA	NVIDIA HPC & IA perspective
Hardware vendors & experts	11:25	00:25	11:50	tbd	IBM	IBM HPC perspective
Hardware vendors & experts	11:50	00:25	12:15	J.Panziera	Atos-BULL	Bull HPC perspective
Academics	12:15	00:20	12:35	S.Petiton	Univ.Lille &MdlS	New methods in Linear algebra & HPC perspective
	12:35	03:25	16:00			*--Free time for lunch and discussion*
Panel	16:00	01:00	17:00			Panel : future HPC architectures & languages & algorithmics & physics
	17:00	00:10	17:10			Wrap-up
	17:10	00:00	17:10			*--End of day 2 / End of Workshop*